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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,880	12/28/2000	Matthew B. Haycock	42390P10353	9417

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2181	5

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,880	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *3 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Drawings

2. The drawings were received on 3 November 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 103

3. Claims 1, 2, 6, 7, 10, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,072,804 to Beyers, Jr. ("Beyers") in view of US Patent Number 5,933,594 to La Joie et al. ("La Joie") and knowledge which is well known in the art.

In reference to Claim 1, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a buffer having at least one trigger; said buffer being able to observe and echo at least one of the signals transmitted on said bus, transmitted into said component, and transmitted out of said component; and wherein said bus is one of a memory bus, a

data bus, an address bus, and a control bus. La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing signals by a monitoring system (analogous to observing and echoing signals) (See Column 2 Lines 34-41) from the external bus; and said bus being one of a data bus, and address bus, and a control bus (See Column 5 Lines 45-50). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

In reference to Claim 2, Beyers, La Joie, and knowledge commonly known in the art teach the limitations as applied to Claim 1 above. Beyers further teaches a bus connected between a port on the analyzer buffer (analogous to the observability bus and observability port) (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control (analogous to the logic analyzer and bus analyzer) (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal (analogous to detecting the signal) (See Column 13 Lines 36-38); defining a data capture window (analogous to accessing the signal) (See Column 14 Lines 13-15); and storing the data in the analyzer buffer (analogous to reading the signal) (See Column 14 Lines 4-5).

In reference to Claim 6, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a buffer having at least one trigger; observing and echoing at least one of the

signals transmitted on said bus, transmitted into the component, and transmitted out of the component; and wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus. La Joie teaches a buffer having a trigger (See Figure 1, Column 13 Lines 58-67, and Column 14 Lines 1-34); capturing signals by a monitoring system (analogous to observing and echoing signals) (See Column 2 Lines 34-41) from the external bus; and said bus being one of a data bus, and address bus, and a control bus (See Column 5 Lines 45-50). The Examiner takes Official Notice that a memory bus is a common component in the hierarchy of busses in a PC used to carry memory addresses and data. This is shown to have been well known in the art at the time the invention was made by The PC Guide (See entry for "The Memory Bus").

In reference to Claim 7, Beyers, La Joie, and knowledge commonly known in the art teach the limitations as applied to Claim 6 above. Beyers further teaches receiving the external signals (See Column 13 Lines 34-36); capturing the external signal (analogous to detecting the signal) (See Column 13 Lines 36-38); defining a data capture window (analogous to accessing the signal) (See Column 14 Lines 13-15); and storing the data in the analyzer buffer (analogous to reading the signal) (See Column 14 Lines 4-5).

In reference to Claim 10, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not teach a memory; an I/O port; a microprocessor; wherein said memory, I/O port, and microprocessor are connected by a data bus, an address bus, and a control bus; and a

buffer means, integrated on a component coupled to one of said busses, for observing and echoing at least one of signals transmitted on a bus, signals transmitted into the component, and signals transmitted out of said component. La Joie teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1 Number 12); and a buffer (See Figure 1 Number 20) that stores data captured from the external bus (analogous to observing and echoing signals) (See Column 14 Lines 1-13). La Joie teaches the processor (See Figure 1 Number 10) being connected by the processor bus to a control interface (See Figure 1 Number 24) which means the bus would necessarily include a control bus, and a memory (See Figure 1 Number 22) which means the bus would necessarily include a data bus and an address bus. La Joie further teaches that common components of busses include address lines, data lines, and control lines (See Column 5 Lines 45-46).

In reference to Claim 11, Beyers and La Joie teach the limitations as applied Claim 10 above. Beyers further teaches receiving the external signals (See Column 13 Lines 34-36); capturing the external signal (analogous to detecting the signal) (See Column 13 Lines 36-38); defining a data capture window (analogous to accessing the signal) (See Column 14 Lines 13-15); and storing the data in the analyzer buffer (analogous to reading the signal (See Column 14 Lines 4-5).

In reference to Claim 14, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5); and wherein signals are transmitted into and out of said component (See Figures 4 and 5). Beyers does not

teach a memory; an I/O port; a microprocessor; wherein said memory, I/O port, and microprocessor are connected by a data bus, an address bus, and a control bus; and a buffer means, integrated on a component coupled to one of said busses, for observing and echoing at least one of signals transmitted on a bus, signals transmitted into the component, and signals transmitted out of said component. La Joie teaches a memory (See Figure 1 Number 22); an I/O port (See Figure 1 Number 28); a microprocessor (See Figure 1 Number 10); a processor bus connecting the memory, I/O port, and microprocessor (See Figure 1 Number 12); and a buffer (See Figure 1 Number 20) that stores data captured from the external bus (analogous to observing and echoing signals) (See Column 14 Lines 1-13). La Joie teaches the processor (See Figure 1 Number 10) being connected by the processor bus to a control interface (See Figure 1 Number 24) which means the bus would necessarily include a control bus, and a memory (See Figure 1 Number 22) which means the bus would necessarily include a data bus and an address bus. La Joie further teaches that common components of busses include address lines, data lines, and control lines (See Column 5 Lines 45-46).

In reference to Claim 15, Beyers and La Joie teach the limitations as applied to Claim 14 above. Beyers further teaches a bus connected between a port on the analyzer buffer (analogous to the observability bus and observability port) (See Figure 1 and Column 14 Lines 4-15) and the analyzer logic control (analogous to the logic analyzer and bus analyzer) (See Figure 1, Column 13 Lines 60-67, and Column 14 Lines 1-4) to receive the signals (See Column 13 Lines 34-36); capturing the external signal (analogous to detecting the signal) (See Column 13 Lines 36-38); defining a data

capture window (analogous to accessing the signal) (See Column 14 Lines 13-15); and storing the data in the analyzer buffer (analogous to reading the signal) (See Column 14 Lines 4-5).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers with the device of La Joie, resulting in the inventions of Claims 1, 2, 6, 7, 10, 11, 14, and 15, in order to monitor the individual components as well as identify and diagnose errors that occur therein (See Column 1 Lines 11-14 of La Joie).

4. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers and La Joie as applied to Claims 2 and 15 above, and further in view of US Patent Number 6,496,583 to Nakamura et al. ("Nakamura").

In reference to Claim 3, Beyers and La Joie teach the limitations as applied to Claim 2 above. Beyers and La Joie do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

In reference to Claim 16, Beyers and La Joie teach the limitations as applied to Claim 15 above. Beyers and La Joie do not teach that the observability port is a logic observability port. Nakamura teaches a device that contains logic ports as an interface (See Figure 8 and Column 2 Lines 57-61).

One of ordinary skill in the art would combine the device of Beyers and La Joie with the device of Nakamura, resulting in the inventions of Claim 3 and 16, in order to

provide a means for converting the data at the port into a format compatible with the bus and devices connected to the port (See Column 3 Lines 23-27 of Nakamura).

5. Claims 4, 8, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers and La Joie as applied to Claims 1, 6, 10, and 14 above, and further in view of US Patent Number 6,147,863 to Moore et al. ("Moore").

In reference to Claim 4, Beyers and La Joie teach the limitations as applied to Claim 1 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

In reference to Claim 8, Beyers and La Joie teach the limitations as applied to Claim 6 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

In reference to Claim 12, Beyers and La Joie teach the limitations as applied to Claim 10 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA

expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

In reference to Claim 17, Beyers and La Joie teach the limitations as applied to Claim 14 above. Beyers and La Joie do not teach the bus being one of a simultaneous bi-directional bus having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. Moore teaches the use of a PCI bus and an ISA bus to transfer data (See Abstract, Column 1 Lines 13-15, and Column 1 Lines 57-67).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Moore, resulting in the inventions of Claims 4, 8, 12, and 17, in order to allow the device to be compatible with a wide range of devices because PCI busses and ISA busses are standardized busses with widespread use.

6. Claims 5, 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyers and La Joie as applied to Claims 1 and 6 above, and further in view of US Patent Number 6,587,679 to Hokao ("Hokao").

In reference to Claim 5, Beyers and La Joie teach the limitations as applied to Claim 1 above. Beyers and La Joie do not teach the buffer being configured to observe and echo signals transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

In reference to Claim 9, Beyers and La Joie teach the limitations as applied to Claim 6 above. Beyers and La Joie do not teach the signals being transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

In reference to Claim 13, Beyers and La Joie teach the limitations as applied to Claim 10 above. Beyers and La Joie do not teach the signals being transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

In reference to Claim 18, Beyers and La Joie teach the limitations as applied to Claim 14 above. Beyers and La Joie do not teach the buffer being configured to observe and echo signals transmitted by wireless communication. Hokao teaches a method of monitoring signals in a wireless communications device (See Abstract and Column 1 Lines 9-11).

One of ordinary skill in the art at the time the invention was made would combine the device of Beyers and La Joie with the device of Hokao, resulting in the inventions of Claims 5, 9, and 14, in order to monitor signals that are communicated wirelessly (See Column 1 Lines 33-38 of Hokao) as well as monitor the signal without affecting it or being detected by the communicating parties.

Response to Arguments

7. Applicant's arguments filed 3 November 2003 have been fully considered but they are not persuasive.

8. Applicant's arguments with respect to Independent Claims 1, 6, 10, and 14, and Dependent Claims 2-5, 7-9, 11-13, and 15-18 have been considered but are moot in view of the new ground(s) of rejection. Applicant has modified the scope of the claims to include the limitation of the buffer being integrated on a component connected to a bus. As shown above, Beyers teaches a component containing a plurality of devices connected with a bus (See Figures 4 and 5) and La Joie teaches a buffer as part of a bus monitoring device (See Figure 1 Number 20). Therefore, the changes are not persuasive to overcome a rejection based on 35 USC § 103. The new ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

9. In response to applicant's argument that Beyers and La Joie are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, although the desired use of the invention of Beyers is directed towards consumer electronic equipment (specifically, video signal processing equipment), the invention as described and claimed is for a data transmission bus

system that includes a plurality of nodes connected by a ring bus. As such, the device is in the same field of endeavor as the computer diagnostic system of La Joie.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
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tjc

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